IN THE CLAIMS

1. (Twice amended) A bonding pad structure of a semiconductor device, said bonding pad structure comprising:

a substructure formed on a semiconductor substrate;

a first dielectric layer formed on the substructure;

a polysilicon film plate formed on the first dielectric layer;

a second dielectric layer formed overlying the polysilicon film plate, the second dielectric layer having a first opening that expose a region of the polysilicon film plate,

a first metal layer formed on the polysilicon film plate through the first opening;

an inter-metal dielectric (IMD) layer formed overlying the first metal layer, the inter-metal dielectric layer having a second opening that exposes a region of the first metal layer;

a second metal layer formed on the first metal layer in the second opening; and

a passivation layer formed overlying the second metal layer, the passivation layer having a third opening that exposes a region of the second metal layer as a bonding pad, the bonding pad directly overlying the polysilicon film plate.

2. (Currently amended) A bonding pad structure according to claim 1, wherein the first metal layer is formed having a somewhat horseshoe-shaped cross-section.

3. (Currently amended) A bonding pad structure according to claim 2, wherein a region of the second metal layer is disposed within a recessed area of the first metal layer.

4. (Currently amended) A bonding pad structure according to claim 1, wherein the second metal layer has a somewhat horseshoe-shaped cross-section.

5. (Currently amended) A bonding pad structure according to claim 1, wherein the substructure comprises circuitry configured to provide a dynamic random access memory.

6. (Currently amended) A bonding pad structure according to claim 1, wherein the first dielectric layer is a boron phosphor silicate glass (BPSG) layer.

7. (Currently amended) A bonding pad structure according to claim 1, wherein the first dielectric layer has a thickness of between about 3000-4000 Å.

8. (Currently amended) A bonding pad structure according to claim 1, wherein the polysilicon film plate has a thickness of about 1000-2000 Å.

9. (Currently amended) A bonding pad structure according to claim 1, wherein the first and second metal layers are formed of aluminum.

10. (Currently amended) A bonding pad structure according to claim 1, wherein the first metal layer has a thickness of approximately 7000-7500 Å.

11. (Currently amended) A bonding pad structure according to claim 1, wherein the second metal layer has a thickness of about 8500-9000 Å.

12. (Currently amended) A bonding pad structure according to claim 1, wherein the wire bonding is beam lead bonding.

13. (Currently amended) A semiconductor package comprising a semiconductor chip having the bonding pad structure of claim 1.

14. (Currently amended) A semiconductor package module having a semiconductor chip mounted thereon, wherein the semiconductor chip comprises a bonding pad structure according to claim 1.

Claims 15-19 are withdrawn.

20. (Twice amended) A bonding pad structure of a semiconductor device, said bonding pad structure comprising:

a substructure formed on a semiconductor substrate;

a first dielectric layer formed on the substructure;

a polysilicon film plate formed on the first dielectric layer and configured to improve the resistance of the bonding pad to stress created during wire bonding;

a first metal layer formed on the polysilicon film plate, wherein the first metal layer is formed having a recessed area;

a second metal layer formed on the first metal layer, wherein a portion of the second metal layer is arranged within the recessed area of the first metal layer to improve the resistance of the bonding pad to stress; and

a passivation layer formed overlying the second metal layer having an opening that exposes a region of the second metal layer as a bonding pad, the exposed region of the second metal layer directly overlying the polysilicon film plate.

Cancel claim 21, without prejudice.

21. (Previously added) A bonding pad according to claim 20, wherein the substructure comprises a gate dielectric layer and a gate electrode sequentially formed on the semiconductor substrate, the substructure includes source/drain regions formed adjacent to the gate electrode.

22. (New) The bonding pad structure according to claim 20, wherein the polysilicon film plate absorbs thermo-mechanical stress induced in the bonding pad during wire bonding.